WHAT IS CLAIMED IS:

1. A current pulse receiving circuit comprising:

a current-to-voltage converter portion that converts an input current pulse to a voltage pulse;

a comparator circuit that compares as an input signal an output signal from the current-to-voltage converter portion with a signal complementary to the output signal or a reference voltage and outputs a logic signal pulse;

a first hysteresis circuit that sets a hysteresis voltage of a first predetermined width to the input signal to the comparator circuit based on the logic signal pulse output therefrom; and,

a second hysteresis circuit that sets a hysteresis voltage that decreases with time from a second predetermined width to the input signal to the comparator circuit based on the logic signal pulse output therefrom.

2. The current pulse receiving circuit according to claim 1, wherein the input current pulse is an output signal from a photodetector.

3. The current pulse receiving circuit according to claim 1, wherein:

the input signal to the comparator circuit is given through a hysteresis resistance component;

the first hysteresis circuit is provided with a first constant current source circuit that allows a first predetermined constant current to flow through the hysteresis resistance component while the comparator circuit is outputting the logic signal pulse; and,

the second hysteresis circuit is provided with a current source circuit that allows a current that decreases with time at a predetermined rate from a second predetermined current to flow through the hysteresis resistance component while the comparator circuit is outputting the logic signal pulse.

4. The current pulse receiving circuit according to claim 3, wherein:

the current source circuit is provided with a second constant current source circuit that outputs the second predetermined current and a shunt circuit that shunts the second predetermined current and lets one of the shunted currents flow through the hysteresis resistance component, and

the shunt circuit decreases at the predetermined rate the amount of current shunted to the hysteresis resistance component.

5. The current pulse receiving circuit according to claim 1, further comprising:

a voltage amplitude limiter circuit that is inserted between the current-to-voltage converter portion and the comparator circuit and that limits a voltage amplitude of an output signal from the current-to-voltage converter portion and outputs the resultant signal to the comparator circuit.

6. The current pulse receiving circuit according to claim 5, wherein:

the voltage amplitude limiter circuit comprises a differential amplifier pair to which the output signal from the current-to-voltage converter portion and the signal complementary to the output signal or the output signal and the reference voltage are input.

7. The current pulse receiving circuit according to claim 1, wherein:

an offset setting circuit that sets an offset value of the input signal to the comparator circuit is provided.

8. The current pulse receiving circuit according to claim 7, wherein:

the offset setting circuit allows a predetermined offset voltage set between the input signals to be adjustable externally.

9. The current pulse receiving circuit according to claim 1, further comprising:

a first buffer circuit that supplies an input signal to the comparator circuit;

a capacitive coupling component that supplies an input signal through capacitive coupling to an input terminal of the first buffer circuit; and

a bias resistance component that is connected between the input terminal of the first buffer circuit and a predetermined potential.

10. The current pulse receiving circuit according to claim 9, wherein:

the first buffer circuit is an emitter-follower circuit.

11. The current pulse receiving circuit according to claim 9, wherein:

the first buffer circuit is a source-follower circuit.

12. The current pulse receiving circuit according to claim 9, further comprising:

the voltage amplitude limiter circuit that supplies an input signal to the first buffer circuit through the capacitive coupling component;

a peak hold circuit that holds an output voltage on a high potential side in the output signal from the current-to-voltage converter portion; and

a low potential level boost circuit that increases the output voltage on the low potential side of the voltage amplitude limiter circuit by a predetermined voltage according to the output voltage from the peak hold circuit.

13. The current pulse receiving circuit according to claim 9, further comprising:

the voltage amplitude limiter circuit that supplies an input signal to the first buffer circuit through the capacitive coupling component;

an integrating circuit that integrates an output signal from the current-to-voltage converter portion; and

a low potential level boost circuit that increases an output voltage on a low potential side of the voltage amplitude limiter circuit by a predetermined voltage according to the output voltage from the integrating circuit.

14. The current pulse receiving circuit according to claim 12, wherein:

the low potential level boost circuit is provided with a second buffer circuit to which an output voltage from either the peak hold circuit or a integrating circuit that integrates an output signal from the current-to-voltage converter portion is input.

15. The current pulse receiving circuit according to claim 14, wherein:

the second buffer circuit is an emitter-follower circuit.

16. The current pulse receiving circuit according to claim 14, wherein:

the second buffer circuit is a source-follower circuit.

17. The current pulse receiving circuit according to claim 9, further comprising:

the voltage amplitude limiter circuit that supplies an input signal to the first buffer circuit through the capacitive coupling component;

a peak hold circuit that holds an output voltage on a high potential side in the output signal from the current-to-voltage converter portion; and

a resistivity automatic adjustment circuit that adjusts a current-to-voltage conversion resistance of the current-to-voltage converter portion according to the output voltage from the peak hold circuit.

18. The current pulse receiving circuit according to claim 9, further comprising:

the voltage amplitude limiter circuit that supplies an input signal to the first buffer circuit through the capacitive coupling component;

an integrating circuit that integrates an output signal from the current-to-voltage converter portion; and a resistivity automatic adjustment circuit that adjusts a current-to-voltage conversion resistance of the current-to-voltage converter portion according to the output voltage from the integrating circuit.

19. The current pulse receiving circuit according to claim 12, wherein:

the peak hold circuit is provided with a voltage follower circuit having a time constant for peak hold sufficiently longer as compared with a response time of peak detection.

20. A current pulse receiving circuit comprising:

a current-to-voltage converter circuit that converts an input current pulse to a voltage pulse;

a large signal detection circuit that detects that a voltage amplitude of an output signal from the current-to-voltage converter circuit is a predetermined amplitude or greater; and

a clamp circuit that reduces a current-to-voltage conversion resistance in the current-to-voltage converter circuit and reduces a clamp level of an output voltage amplitude according to an output signal from the large signal detection circuit.

21. The current pulse receiving circuit according to claim 20, wherein:

the input current pulse is an output signal from a photodetector.

22. The current pulse receiving circuit according to claim 20, further comprising:

a DC cancellation circuit that cancels a DC offset component in the current-to-voltage converter circuit, wherein an effect of canceling the DC offset component in the DC cancellation circuit is reduced according to an output signal from the large signal detection circuit.

23. The current pulse receiving circuit according to claim 20, wherein:

the current-to-voltage converter circuit is provided with a current-to-voltage conversion resistance component, and

the clamp circuit is provided with a bias circuit and an emitter-follower transistor or a diode that is connected in parallel with the current-to-voltage conversion resistance component and biased to a conductive state by the bias circuit according to an output signal from the large signal detection circuit.

24. The current pulse receiving circuit according to claim 23, wherein:

the bias circuit has temperature characteristics that suppress temperature characteristics of the emitter-follower transistor or the diode.

25. The current pulse receiving circuit according to claim 20, wherein:

the current-to-voltage converter circuit has a differential input configuration and is provided with a dummy load connected to a non-input terminal.

26. The current pulse receiving circuit according to claim 20, wherein:

the large signal detection circuit is provided with a time constant circuit that outputs an output signal when the voltage amplitude of the output signal from the current-to-voltage converter circuit is a predetermined amplitude or more for a predetermined period of time.

27. A current pulse receiving circuit comprising:

a current-to-voltage converter circuit that converts an input current pulse to a voltage pulse;

an amplifier circuit of a differential input configuration that performs amplification according to an output signal from the current-to-voltage converter circuit;

a buffer circuit of a differential output configuration that is inserted between the current-to-voltage converter circuit and the amplifier circuit; and

a differentiating circuit that differentiates an inverted output from the buffer circuit and supplies this differentiated inverted output to a node having a high impedance of the other input signal lines in the amplifier circuit.

28. The current pulse receiving circuit according to claim 27, further comprising:

a pair of buffer circuits that supply each of input signals to the amplifier circuit; and

the differentiating circuit that differentiates at least one of the inverted outputs of the pair of buffer circuits and supplies this differentiated inverted output to an input signal for the other buffer circuit.

29. The current pulse receiving circuit according to claim 27,

further comprising:

the pair of buffer circuits; and

a pair of differentiating circuits that differentiate each of the inverted outputs from the pair of buffer circuits, wherein the pair of differentiating circuits are disposed symmetrically.

30. The current pulse receiving circuit according to claim 27, further comprising:

a capacitive coupling component that supplies an input signal to the amplifier circuit through capacitive coupling; and wherein

the buffer circuit is provided with an emitter-follower transistor and a constant current source circuit which is connected to an emitter terminal of the emitter-follower transistor and which supplies a bias current; and

the differentiating circuit is provided with a differentiating resistance component that is connected between a collector terminal of the emitter-follower transistor and a predetermined potential and a differentiating capacitive component that is connected between the collector terminal and the other input signal line.

31. The current pulse receiving circuit according to claim 27, further comprising:

a capacitive coupling component that supplies an input signal to the amplifier circuit through capacitive coupling; and wherein

the buffer circuit is provided with a source-follower transistor and a constant current source circuit which is connected to a source terminal of the source-follower transistor and which supplies a bias current; and the differentiating circuit is provided with a differentiating resistance component that is connected between a drain terminal of the source-follower transistor and a predetermined potential and a differentiating capacitive component that is connected between the drain terminal and the other input signal line.

32. The current pulse receiving circuit according to claim 20, further comprising:

an automatic threshold value adjustment circuit or an automatic gain adjustment circuit that limits the output signal from the current-to-voltage converter circuit to within a predetermined voltage amplitude range.